Attorney Docket No. 069974-0143

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S): Keiichiro KATA, et al.

Title: PROCESS FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR WAFER

Original Patent Number: 5,844,304

Original Patent Issue Date: December 1, 1998

Examiner: Unassigned

Art Unit: Unassigned

CONSENT OF ASSIGNEE FOR REISSUE APPLICATION

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Filed herein is a statement under 37 C.F.R. 3.73(b) certifying that NEC Electronics Corp. is the assignee of the entire right, title, and interest in the patent application identified above.

NEC Electronics Corp., the assignee owning an undivided interest in the original patent identified above, consents to the accompanying application for reissue.

The undersigned is empowered to sign this consent on behalf of the assignee.

NEC ELECTRONICS CORP.

Date: July 15, 2003

By: Name: Masahiko Fujiwara
Title: General Manager, Intellectual Asset Division

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CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Commissioner for Patents
Box REISSUE
Washington, D.C. 20231

Dear Sir:

NEC Electronics Corp. certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of an assignment from the inventor of the patent identified above to NEC Corporation, which was recorded in the U.S. Patent and Trademark Office at Reel 7797, Frame 0511 on September 25, 1995, and a subsequent assignment from NEC Corporation to NEC Electronics Corp., which was submitted for recordation on February 25, 2003. Copies both assignments are attached.

The undersigned is empowered to sign this certificate on behalf of the assignee.

NEC ELECTRONICS CORP.

Date: July 15, 2003

By: Name: Masahiko Fujiwara
Title: General Manager, Intellectual Asset Division

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re reissue patent application of

Keiichiro KATA, et al.

Serial No.: **Not Yet Assigned**

Application for reissue of U.S. Patent No. 5,844,304, granted Dec. 1, 1998

Filed: **Herewith**

For: **PROCESS FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR WAFER**

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175 AND POWER OF ATTORNEY

Commissioner for Patents
Box REISSUE
Washington D.C. 20231

Sir:

We, Keiichiro Kata and Shinichi Chikaki, declare that:

1. Our residences, post office addresses, and citizenship are stated below next to our names.

2. We believe that we are the original, first inventors and joint inventors of the subject matter described and claimed in our U.S. Patent No. 5,844,304 and in the foregoing specification for which a reissue patent is sought on the invention entitled PROCESS FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR WAFER, the specification of which is attached hereto.

3. We have reviewed and understand the contents of the above identified specification, including the amended and new claims specifically referred to in this declaration.

4. We acknowledge the duty to disclose information that is material to examination of the application in accordance with 37 C.F.R. § 1.56.

5. We claim priority under 35 U.S.C. § 119 to Japanese patent application 6-237653, filed September 30, 1994.

6. We believe that U.S. Patent No. 5,844,304 may be wholly or partly inoperative or invalid by reason of claims 3 and 4 potentially being interpreted in a manner that is broader than intended and by reason of our patent having less specific claim coverage in the form of dependent claims than we had a right to claim..

7. At least one error was not to include the clarifying amendments to claims 3 and 4 as contained in the Preliminary Amendment filed concurrently herewith and provided below:

3. (Amended) A semiconductor wafer including:

a plurality of chip sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes, wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein <u>said aluminum layer and said plating extend from one of said bump electrodes to one of said chip electrodes and</u> said plating contacts <u>said</u> one of said bump electrodes and said aluminum layer contacts <u>said</u> one of said chip electrodes.

4. (Amended) A semiconductor wafer including:

a plurality of chip sections defined thereon by scribe lines, each chip section having:

bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein said aluminum layer and said plating extends from one said bump electrode to one of said chip electrodes and said plating contacts said one of said bump electrodes and said aluminum layer contacts said one of said chip electrodes.

8. At least one error was not to include new dependent claims in the Preliminary Amendment filed concurrently herewith and provided below:

13. (New) The semiconductor wafer of claim 1, wherein the plurality of chip electrodes are positioned on said periphery.

14. (New) The semiconductor wafer of claim 2, wherein the plurality of chip electrodes are positioned on said periphery.

15. (New) The semiconductor wafer of claim 3, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

16. (New) The semiconductor wafer of claim 4, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

17. (New) The semiconductor wafer of claim 1, wherein said bump electrodes overlap said chip electrodes.

18. (New) The semiconductor wafer of claim 2, wherein said bump electrodes overlap said chip electrodes.

19. (New) The semiconductor wafer of claim 3, wherein said bump electrodes overlap said chip electrodes.

20. (New) The semiconductor wafer of claim 4, wherein said bump electrodes overlap said chip electrodes.

21. (New) The semiconductor wafer of claim 1, wherein said bump electrodes do not overlap said chip electrodes.

22. (New) The semiconductor wafer of claim 2, wherein said bump electrodes do not overlap said chip electrodes.

23. (New) The semiconductor wafer of claim 3, wherein said bump electrodes do not overlap said chip electrodes.

24. (New) The semiconductor wafer of claim 4, wherein said bump electrodes do not overlap said chip electrodes.

25. (New) A semiconductor wafer of claim 1, wherein said bump electrodes are arranged in a grid array.

26. (New) The semiconductor wafer of claim 2, wherein said bump electrodes are arranged in a grid array.

27. (New) The semiconductor wafer of claim 3, wherein said bump electrodes are arranged in a grid array.

28. (New) The semiconductor wafer of claim 4, wherein said bump electrodes are arranged in a grid array.

29. (New) The semiconductor wafer of claim 1, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

30. (New) The semiconductor wafer of claim 2, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

31. (New) The semiconductor wafer of claim 3, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

32. (New) The semiconductor wafer of claim 4, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

9. All errors that are being corrected up to the time of the filing of the Declaration in this reissue application arose without any deceptive intent on our part.

WHEREFORE, Petitioner prays that Petitioner may be allowed to surrender the original Letters Patent 5,844,304 and do hereby offer the same.

APPLICANTS HEREBY APPOINT the registered attorneys and agents at Customer Number 22428

FOLEY & LARDNER
Customer Number: 22428
22428
22428
PATENT TRADEMARK OFFICE

to have full power to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent, and to transact all business in the United States Patent and Trademark Office connected therewith, and requests that all correspondence be sent to FOLEY & LARDNER, 3000 K Street, N.W., Suite 500, Washington, DC 20007-5109 at (202) 672-5300.

The undersigned hereby declares further that all statements made herein of his or her own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title

18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Keiichiro Kata

Signature: Keiichiro Kata *Date:* July 17, 2003

Residence: Kanagawa, Japan

Post Office Address: c/o NEC Electronics Corp. *Citizenship:* Japan
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Shinichi Chikaki

Signature: Shinichi Chikaki *Date:* July. 17. 2003

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